What is claimed is:

1. A semiconductor device comprising:

a layer of a second conductivity, formed on top of a substrate of a first conductivity;

a layer of the first conductivity, formed inside the layer of the second conductivity;

a source electrode formed in a trench cavity surrounded by a first heavily doped region of the second conductivity, inside the layer of the first conductivity;

a drain electrode formed in a trench cavity surrounded by a second heavily doped region of the second conductivity, inside the layer of the second conductivity; and

a gate electrode formed in at least one of trench cavities, having a sidewall in contact with the first heavily doped region, located on one edge of the layer of the first conductivity and between the source electrode and the drain electrode, through the intermediary of an oxide film covering the inner surface of the trench cavities.

2. A semiconductor device comprising:

a layer of a second conductivity, formed on top of an insulating oxide film layer of a SOI substrate with a substrate of a first conductivity type, serving as a support substrate thereof;

a layer of the first conductivity, formed so as to be adjacent to the layer of the second conductivity, and on top of the insulating oxide film layer of the SOI substrate;

a source electrode formed in a trench cavity surrounded by a first heavily doped region of the second conductivity, inside the layer of the first conductivity;

a drain electrode formed in a trench cavity surrounded by a second heavily doped region of the second conductivity, inside the layer of the second conductivity; and

a gate electrode formed in at least one of trench cavities, having a sidewall in contact with the first heavily doped region, located on one edge of the layer of the first conductivity and between the source electrode and the

drain electrode, through the intermediary of an oxide film covering the inner surface of the trench cavities.

3. A semiconductor device according to claim 1, wherein a plurality of the trench cavities for the gate electrodes are disposed in a line in the direction of a channel width.

4. A semiconductor device according to claim 1, wherein the trench cavities for the gate electrodes are substantially in the shape of a column.

5. A semiconductor device according to claim 1, wherein impurity concentration of the layer of the first conductivity is higher than that of the layer of the second conductivity.

6. A semiconductor device according to claim 1, wherein a heavily doped region of the first conductivity type is formed within the layer of the first conductivity to take out a potential of the layer of the first conductivity.

7. A semiconductor device according to claim 1, wherein the trench cavities for the gate electrodes have a depth equal to a depth of the first heavily doped region surrounding the trench cavity for the source electrode.

8. A process of fabricating a semiconductor device, comprising:

forming a layer of a second conductivity, on top of a substrate of a first conductivity;

forming a layer of the first conductivity, inside the layer of the second conductivity;

forming two trench cavities one of which is located on one edge of the layer of the first conductivity, adjacent to the layer of the second conductivity, inside the layer of the first conductivity, and forming one trench cavity inside the layer of the second conductivity;

forming an oxide film on the inner surface of the trench cavity of the two trench cavities formed inside the layer of the first conductivity, formed so as to be closer to the layer of the second conductivity;

forming electrode metals to serve as a gate electrode, source electrode, and drain electrode, in the trench cavity with the oxide film formed therein, the other trench cavity formed inside the layer of the first conductivity, and the trench cavity formed inside the layer of the second conductivity, in that order, respectively, and

forming a first heavily doped region of the second conductivity around the source electrode, so as to be in contact with a sidewall of the trench cavity for the gate electrode, and forming a second heavily doped region of the second conductivity around the drain electrode.

9. A process of fabricating a semiconductor device according to claim 8, wherein a plurality of the trench cavities for the gate electrodes are formed so as to be arranged in a line in the direction of a channel width.

10. A process of fabricating a semiconductor device according to laim 8, wherein the trench cavity for the gate electrode is formed substantially in the shape of a column.

11. A process of fabricating a semiconductor device according to claim 8, wherein the trench cavity for the gate electrode is formed such that a depth thereof is equal to a depth of the first heavily doped region surrounding the trench cavity for the source electrode.

12. A process of fabricating a semiconductor device according to claim 8, wherein a distance between the sidewall of the trench cavity for the gate electrode and the second heavily doped region of the second conductivity, surrounding the trench cavity for the drain electrode, is set in such a way as to be able to obtain a drain voltage resistance as desired.

13. A process of fabricating a semiconductor device, comprising:

forming a layer of a second conductivity, on top of an insulating oxide film layer of a SOI substrate provided with a substrate of a first conductivity type, serving as a support substrate;

forming a layer of the first conductivity on top of the insulating oxide film layer of the SOI substrate, so as to be adjacent to the layer of the second conductivity, and;

forming two trench cavities one of which is located on one edge of the layer of the first conductivity, adjacent to the layer of the second conductivity, inside the layer of the first conductivity, and forming one trench cavity inside the layer of the second conductivity;

forming an oxide film on the inner surface of the trench cavity of the two trench cavities formed inside the layer of the first conductivity, formed so as to be closer to the layer of the second conductivity;

forming electrode metals to serve as a gate electrode, source electrode, and drain electrode, in the trench cavity with the oxide film formed therein, the other trench cavity formed inside the layer of the first conductivity, and the trench cavity formed inside the layer of the second conductivity, in that order, respectively, and

forming a first heavily doped region of the second conductivity around the source electrode, so as to be in contact with a sidewall of the trench cavity for the gate electrode, and forming a second heavily doped region of the second conductivity around the drain electrode.

14. A process of fabricating a semiconductor device according to claim 13, wherein a plurality of the trench cavities for the gate electrodes are formed so as to be arranged in a line in the direction of a channel width.

15. A process of fabricating a semiconductor device according to claim 13, wherein the trench cavity for the gate electrode is formed substantially in the shape of a column.

16. A process of fabricating a semiconductor device according to claim 13, wherein the layer of the first conductivity is formed such that impurity concentration thereof is higher than that of the layer of the second conductivity.

17. A process of fabricating a semiconductor device according to claim 13, wherein the trench cavity for the gate electrode is formed such that a depth thereof is equal to a depth of the first heavily doped region surrounding the trench cavity for the source electrode.

18. A process of fabricating a semiconductor device according to claim 13, wherein a distance between the sidewall of the trench cavity for the gate electrode and the second heavily doped region of the second conductivity, surrounding the trench cavity for the drain electrode, is set in such a way as to be able to obtain a drain voltage resistance as desired.